ALTERNATE SET OF REGISTERS FOR SPEEDING THE SERVICE OF CRITICAL INTERRUPTS AND OPERATING SYSTEM TRAPS

Philip A. Bourekas

ABSTRACT

A processor includes a set of general purpose registers that are used when executing generic tasks and a set of exception registers that is dedicated for servicing specific exceptions. When a task is interrupted with an asserted "fast" exception, the processor automatically diverts the exception to the dedicated exception registers using a dedicated vector. The dedicated vector and exception registers may be reserved for high priority, i.e., critical, exceptions. Because the exception registers are automatically activated for fast exceptions, there is no need to determine the priority of the exception. Further, high priority interrupts and high priority operating system calls (traps) may have different dedicated vectors and the set of exception registers may have a portion allocated for servicing interrupts and another portion allocated for servicing operating system calls. With the use of a dedicated vector or dedicated vectors, there is no need for software to decode the fast exception. Advantageously, during the servicing of the exception, the values of the exception registers may be modified, without disrupting the state of the interrupted task. Thus, because a set of dedicated exception registers are swapped in for the general purpose registers to service an exception, there is no need for explicit state management prior to or after servicing the exception.